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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-------------------------------|-------------|----------------------|---------------------|------------------|
| 09/253,995 | 02/22/1999 | YOSHIHIRO SAGA | B208-1021 | 6335 |
| 26272 | 7590 | 10/20/2005 | EXAMINER | |
| COWAN LIEBOWITZ & LATMAN P.C. | | | HANNETT, JAMES M | |
| JOHN J TORRENTE | | | ART UNIT | |
| 1133 AVE OF THE AMERICAS | | | PAPER NUMBER | |
| NEW YORK, NY 10036 | | | 2612 | |

DATE MAILED: 10/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/253,995

Applicant(s)

SAGA, YOSHIHIRO

Examiner

James M. Hannett

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 March 2005.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 41, 43 and 47-55 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 41, 43 and 47-55 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 22 February 1999 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The final rejection mailed 7/27/2005 inadvertently did not contain the Final Office action and instead contained the previous Non-Final Office action. Therefore, the Final Office action is being re-mailed and the statutory period for reply is set to expire 3 months from the mailing date of this action.

Response to Arguments

Applicant's arguments filed 3/21/2005 have been fully considered but they are not persuasive. The applicant argues that the prior art does not teach the new limitation of a display for displaying an image using the image data stored in memory. Furthermore, the applicant argues that the prior art does not teach the new limitation of assigning a higher priority to a process of providing image data from the memory to the image display unit than a process of refreshing the memory. The examiner disagrees with the applicants arguments and refers the applicant to the following office action for the examiners response to arguments.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1: Claims 41, 43, 47-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 5,146,592 Pfeiffer et al in view of USPN 5,826,035 Hamada et al.

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2: As for Claim 41, Pfeiffer et al teaches in Figure 1 the use of an image capture apparatus comprising: an image capture unit (10) adapted to capture image data, Column 5, Lines 58-66. Pfeiffer et al teaches that the image capture apparatus has storage means (84) for storing image data. Pfeiffer et al further teaches on Column 38, Lines 19-30, Column 23, Lines 20-34 and Column 23, Lines 24-32 that the parallel image processor (72) can perform image processing in the image data (84) in parallel with the process of displaying an image on the display (color monitor). Pfeiffer et al teaches that the image algorithm processor is the master controller of the image computer, providing addresses for the image memory and thus data for the parallel image processor set in carrying out data processing tasks. The image algorithm processor (66) is viewed by the examiner as the control unit. Pfeiffer et al teaches on Column 22, Lines 33-40 that the image capture apparatus has a video DRAM refresh controller having a number of programmable registers for defining the various timing constraints and operations of the controller. Pfeiffer et al teaches on Column 23, Lines 20-34 that the image processing apparatus is capable of performing a process of screen refresh and a process of the image algorithm processor and states that both processes can access the image memory. Pfeiffer et al teaches on Column 23, Lines 24-32 that an arbitration circuit is provided to determine the priority of the various requests to access memory. Pfeiffer et al teaches that the screen refresh function of the video DRAM shift registers is given top priority (which is viewed as the process of storing the image data), followed by refresh of the DRAM cells, and then address request from the image algorithm processor. The examiner views the image capture unit as being the combination of the video image transducer and the digitizer and mass storage (18). As depicted in Figure 1, the video image computer controls the image capture unit. Therefore, the video image computer is

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viewed by the examiner as the control unit adapted to control the image capture apparatus using the memory. Therefore, when the image computer receives a request to refresh the video screen with new data, the memory that is digitized in the image capture unit (10 and 18) is read via the data bus unit to the image memory (84). This process is viewed by the examiner as a process of providing image data from the image capture unit to the memory. Pfeiffer et al teaches providing image data from the memory (84) to the image algorithm processor for image processing.

Pfeiffer et al teaches that the screen refresh function of the video DRAM shift registers is given top priority (which is viewed as the process of storing the image data), followed by refresh of the DRAM cells, and then address request from the image algorithm processor. Pfeiffer et al teaches on Column 23, Lines 24-32 and depicts in Figure 1 and 3 an image display unit (28) adapted to display the image data stored in memory (82) on display apparatus (28), Pfeiffer et al teaches that the screen refresh function of the video DRAM shift registers is given top priority (which is viewed as the process of storing the image data), followed by refresh of the DRAM cells.

Therefore, the arbitration unit also adapted to assign a higher priority to a process of providing image data from the memory to the image display unit than a process of refreshing the memory.

However, Pfeiffer et al does not teach that the image algorithm processor can perform a compression and expansion function.

Hamada et al teaches on Column 9, Lines 44-57 the use of including compression and expansion algorithms in an image processor in order to allow image data to be stored in a smaller required memory size.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include compression and expansions capabilities as taught by Hamada et

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al in the image algorithm processor of Pfeiffer et al in order to allow the image data to be stored in a reduced memory size.

3: In regards to Claim 43, Pfeiffer et al teaches that the image processing system includes an image capture unit (10) adapted to capture image data. Therefore, the system as taught by Pfeiffer et al is viewed as a digital camera.

4: As for Claim 47, Pfeiffer et al teaches on Column 23, Lines 20-34 and Column 5, Lines 58-66 an image processing unit adapted to process the image data stored in the memory (82).

5: In regards to Claim 48, Pfeiffer et al teaches on Column 23, Lines 20-34 and Column 23, Lines 24-32 that an arbitration circuit is provided to determine the priority of the various requests to access memory. Pfeiffer et al teaches that the screen refresh function of the video DRAM shift registers is given top priority (which is viewed as the process of storing the image data), followed by refresh of the DRAM cells, and then address request from the image algorithm processor. Therefore, Pfeiffer et al teaches providing image data from the memory (84) to the image algorithm processor for image processing. Pfeiffer et al teaches the method of assigning a higher priority to a process that the control unit uses the memory (screen refresh) than a process of providing image data from the memory to the image algorithm processor. It is inherent that a predetermined amount of time would elapse after the memory is refreshed.

6: As for Claim 49, Pfeiffer et al teaches that the screen refresh function of the video DRAM shift registers is given top priority (which is viewed as the process of storing the image data), followed by refresh of the DRAM cells, and then address request from the image algorithm processor. However, Pfeiffer et al does not teach that the image algorithm processor can perform a compression and expansion function.

Hamada et al teaches on Column 9, Lines 44-57 the use of including compression and expansion algorithms in an image processor in order to allow image data to be stored in a smaller required memory size.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include compression and expansions capabilities as taught by Hamada et al in the image processor of Pfeiffer et al in order to allow the image data to be stored in a reduced memory size. The compression and expansion capabilities of Hamada et al are viewed by the examiner a process of processing the image data by changing a size of the image data.

7: In regards to Claim 50, Pfeiffer et al depicts in Figure 1 that the image capture system includes an image capture unit (10 and 18) adapted to capture image data. Therefore, the system as taught by Pfeiffer et al is viewed as a digital camera.

8: As for Claim 51, Pfeiffer et al teaches on Column 23, Lines 20-34 Pfeiffer et al teaches on Column 23, Lines 24-32 that an arbitration circuit is provided to determine the priority of the various requests to access memory. Pfeiffer et al teaches that the screen refresh function of the video DRAM shift registers is given top priority (which is viewed as the process of storing the image data), followed by refresh of the DRAM cells, and then address request from the image algorithm processor. Therefore, Pfeiffer et al teaches providing image data from the memory (84) to the image algorithm processor for image processing. Pfeiffer et al teaches the method of assigning a higher priority to a process that the control unit uses the memory (screen refresh) than a process of providing image data from the memory to the image algorithm processor which performs compression in view of Hamada et al. It is inherent that a predetermined amount of time would elapse after the memory is refreshed.

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9: In regards to Claim 52, Pfeiffer et al depicts in Figure 1 that the image processing system includes an image capture unit (10 and 18) adapted to capture image data. Therefore, the system as taught by Pfeiffer et al is viewed as a digital camera.

10: As for Claim 53, Pfeiffer et al further teaches on Column 38, Lines 19-30, Column 23, Lines 20-34 and Column 23, Lines 24-32 the image capture apparatus is capable of performing a process of displaying an image using the image data stored in memory (82). Furthermore, Pfeiffer et al teaches that during a blanking period of the display the image algorithm processor (66) will get address requests for the parallel image processor (72). Pfeiffer et al teaches that the parallel image processor (72) can perform image processing in parallel with the process of displaying an image on the display. Furthermore, in view of Hamada as stated above, the parallel image processor can perform image compression. This is viewed by the examiner as a process of changing the size of the image data stored in the memory (82).

11: In regards to Claim 54, Pfeiffer et al depicts in Figure 1 that the image processing system includes an image capture unit (10 and 18) adapted to capture image data. Therefore, the system as taught by Pfeiffer et al is viewed as a digital camera.

12: As for Claim 55, Pfeiffer et al teaches on Column 26, Lines 50-68 that the refresh control unit is adapted to refresh the memory in a blanking period.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO**

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MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Hannett whose telephone number is 571-272-7309. The examiner can normally be reached on 8:00 am to 5:00 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on 571-272-7308. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James M. Hannett
Examiner
Art Unit 2612

JMH
October 17, 2005


NGOC-YEN VU
PRIMARY EXAMINER